1

PROJECT PROGRESS REPORT III

For The Project Of

LOCALLY CONNECTED ADAPTIVE GABOR FILTER FOR REAL-TIME MOTION COMPENSATION

For the Period from April 20th of 1994 to July 19th of 1994

This Report Is Submitted to ONR

July 19th, 1994

Principal Investigator: Professor Hua Li
Computer Science Department, College of Engineering
Texas Tech University, Lubbock, TX 79409
Telephone: (806) 742-3513, E-mail: xdhua@ttacs1.ttu.edu

Administrative Point of Contact
Kathleen Harris, Ph.D., Director of
The Office of Research Services
Texas Tech University
Lubbock, Tx 79409
Phone: (806) 742-3884

PROJECT PROGRESS REPORT III

For The Project Of

LOCALLY CONNECTED ADAPTIVE GABOR FILTER FOR REAL-TIME MOTION COMPENSATION

For the Period from April 20th of 1994 to July 19th of 1994

Accesion For	
NTIS CRA&I	√
DTIC TAB	
Unannounced	
Justification	
By A275175	
Distribution /	
Availability Codes	
Dist	Avail and / or Special
A-1	

This Report Is Submitted to ONR

July 19th, 1994

Principal Investigator: Professor Hua Li
Computer Science Department, College of Engineering
Texas Tech University, Lubbock, TX 79409
Telephone: (806) 742-3513, E-mail: xdhua@ttacs1.ttu.edu

Administrative Point of Contact
Kathleen Harris, Ph.D., Director of
The Office of Research Services
Texas Tech University
Lubbock, Tx 79409
Phone: (806) 742-3884

The Progress Report

This report is the third quartly report for the project of "*locally connected adaptive Gabor filter for real-time motion compensation,*" with grant number N00014-94-1-0077, which has been in the process since October 20th of 1993 and which has been conducted under the supervision of the principal investigator, Professor Hua Li of Texas Tech University.

As at the third quart of year 1, the project has been making progress as planned in the project proposal, 1(b) on page 21. In particular, the following work has been accomplished as itemized below:

1. The software has been developed to implement the Gabor motion detection algorithm. This software consists of utility functions, algorithm modules, and test pattern generators for the experiments and verification of the *spatial* and *temporal selectivity.* A software program manual now is under developing. A fully tested , documented program will be provided at the end of year 1 project.

   In particular, the software package will consist of the following programs:

   (a) Programs for algorithm implementation, which include:

      i. Real Gabor kernel generation with user-selectable kernel size, spatial frequency, and orientation frequency;
      ii. Imaginary Gabor kernel generation with user-selectable kernel size, spatial frequency, and orientation frequency;
      iii. Image convolution program with user-selectable kernels;
      iv. Least square estimation algorithm for solving an over-determined linear system, which is needed at the last phase for optical flow computation.

   (b) Utility programs which consist of

      i. The program generating test image patterns. The program allows user to define the observer's position (camera position), the fixation direction of the camera, and the orientation of the projection plane (virtual film.) It also allows the user to define objects in three-dimensional world-coordinated system.
      ii. The program creating animated images. The program will produce each individual frame of images, and generate a animated image sequence. These two programs will be particularly needed to test and verify the

optical flow computation based on the generated known motion of the images.

iii. The program creating postscript files. This will produce the hardcopy of images, and computation result.

2. Based on the theoretical analysis, the optical flow was computed for several artificially generated test patterns. These test patterns are designed to test the concept of *spatial* and *orientation selectivity* The patterns were generated by using *virtual reality* technique based on *three-dimensional computer graphics.* As described in the second quartly report, they include stationary observer while object is moving, and stationary object while observer is moving, as well as both observer and object moving in a known fashion. In order to further test the computation, we have modified the resolution and color depth of each pixel to make them all 120-by-100 in resolution and 8-bit color per pixel. A set of floppy disks are now prepared for the demonstration purpose. This set of floppy disks will be provided to ONR once fully tested. Included in this set of disks are image sequences generated under known conditions as benchmark for the future testing of VLSI implementation, in particular, they include the following:

   (a) An observer (camera) is stationary, but the viewing object (a sphere with radius equal to 25 units) is moving along y-axis 5 units per frame.

   (b) The observer is moving along y-axis 5 units per frame while the viewing object is stationary.

   (c) Both the observer and the viewing object are moving 5 units along y-axis and z-axis respectively.

3. In addition to the algorithm development and verification, we have also started work on the design and verification of the electronics basic building blocks for the VLSI implementation. This early start of the hardware design concurrent with the algorithm analysis and verification will further ensure the quality of the work in both hardware and software. In particular, the work in VLSI implementation at this stage includes

   (a) Design one of the most essential building blocks, a video frequency opAmp. With extensive SPICE simulations using the device model provided from MOSIS actual fabrication run, we have completed the design. The characteristics

of the OpAmp to be used to build two-dimensional convolution unit is given in a research memo and was included in the 2nd quart report as Appendix II.

(b) Design analog multiplier, which is to be used for building two-dimensional analog convolution unit. Extensive SPICE simulation was performed. The preliminary simulation data looks very positive and the circuit layout design was started.

(c) Post-layout SPICE simulation is under way to check the actual VLSI implementation. The result will be documented and reported accordingly.

4. In order to benchmark the VLSI chips, a hardware prototype board is under design and construction. This board will be used to compare the performance of digital approach vs. analog approach, analog approach based on the standard off-the shelf components vs. analog customer-design VLSI approach. The board is to be operating in the 4th quarter. The board is designed with a 486 machine as a host. The prototype demonstration will be scheduled with ONR.

As briefly summaried here, the project has been making progress as planned. In the next phase, at the end of one year of the project, we plan to report our progress with software manual, demonstration program, and prototype board demonstration.

The End.